Notice of Allowability	Application No.	Applicant(s)	
	09/656,582	DAVIS ET AL.	
	Examiner	Art Unit	
	Phuong N. Hoang	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/30/04*.

2. ☒ The allowed claim(s) is/are *1 - 2, 6 - 14, 18, 21, 23 - 28, 30 - 37; now renumbered as 1 - 27*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☒ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. James A. Lucas (Reg. No. 21,081) on July 30, 2004.

3. The application has been amended as follows:

In the claims:

a. Claim 1,

(i) at line 8, insert after "coprocessors" -- , wherein the coprocessors are selected from the group including a tree search coprocessor, a checksum coprocessor, a stringcopy coprocessor, an enqueue coprocessor, a datastore coprocessor, a CAB coprocessor, a counter coprocessor and a policy coprocessor, and wherein one of the arbiters is a coprocessor execution interface arbiter to determine the priority between multiple code threads --.

b. Cancel claim 3;

c. Cancel claim 4;

d. Cancel claim 5;

e. Claim 6,

(i) at line 1, replace "3" with -- 1 --;

f. Claim 9,

(i) at line 3, insert after "said" -- embedded processor --;

(ii) at line 7, insert after "the" – network processing --;

(iii) at line 10, insert after "coprocessors" -- , wherein the network processing system including specific operating instructions executed by the threads of the CLPs which result in commands to control coprocessor operation, which commands flow through the interface between the CLPs and the coprocessors, and wherein the instructions serve to enable conditional execution of specific coprocessor operations --;

g. Cancel claim 15;

h. Cancel claim 16;

i. Cancel claim 17;

j. Claim 18,

(i) at line 5, replace "comprising the use by each PPU of a plurality of coprocessors" with – wherein the threads are used by each of said PPUs - -;

(ii) at line 6, replace "the user of" with – used by --;

(iii) at line 6, insert after "interfaces" – coupled to said plurality of coprocessors --;

(iv) at line 8, insert after "coprocessors" -- , and including the use of dedicated coprocessors that support the multiple code threads of the PPU, and wherein one or more of the coprocessors are selected from the group including a tree search coprocessor, checksum coprocessor, stringcopy coprocessor, enqueue coprocessor, datastore coprocessor, CAB coprocessor, counter coprocessor and policy coprocessor, and wherein a coprocessor data interface arbiter serves to determine the priority between data threads --;

k. Cancel claim 19;

l. Cancel claim 20;

m. Claim 21,

(i) at line 1, replace "20" with – 18 --;

n. Cancel claim 22;

o. Claim 23,

(i) at line 1, replace "20" with – 18 --;

p. Cancel claim 29;

q. Claim 30,

(i) at line 2, insert after "each" – of said --;

(ii) at line 2, insert after "processor" – s --;

r. Add new claim 32,

32. In the operation of an embedded processor complex for controlling the programmability of a network processor, the processor complex including a plurality of protocol processor units (PPUs), each PPU containing multiple core language processors (CLPs), each CLP having at least two code threads, each PPU utilizing a plurality of coprocessors useful for executing specific tasks for the PPU, multiple logical

coprocessor interfaces to provide access between each CLP and the coprocessors, and two arbiters between the CLPs and the coprocessors, wherein the coprocessors are selected from the group including a tree search coprocessor, a checksum coprocessor, a stringcopy coprocessor, an enqueue coprocessor, a datastore coprocessor, a CAB coprocessor, a counter coprocessor and a policy coprocessor, and wherein one of the arbiters is a coprocessor data interface arbiter that determines the priority between data threads.

s. Add new claim 33,

33. In the operation according to claim 32 further including a FIFO buffer between each CLP and at least one coprocessor.

t. Add new claim 34,

34. In the operation according to claim 33, wherein the FIFO buffer is between each CLP and the counter coprocessor.

u. Add new claim 35,

35. In the operation according to claim 33, wherein the FIFO buffer is between each CLP and the policy coprocessor.

v. Add new claim 36,

36. A network processing system including an embedded processor embedded processor complex for controlling the programmability of a network processor, said complex including a plurality of protocol processor units (PPUs), each of said PPUs containing:

a) at least two core language processors (CLPs), each CLP having at least two code threads;

b) a plurality of coprocessors for executing specific tasks for the network processing system,

c) multiple coprocessor interfaces to access and share the resources of the coprocessors with each CLP, and

d) two arbiters between the CPLs and the coprocessors,

and wherein the network processing system including specific operating instructions executed by the threads of the CLPs which result in commands to control coprocessor operation, which commands flow through the interface between the CLPs and the coprocessors, and wherein the instructions enable the system to identify long latency events and short latency events according to the expected response time to access data in response to a particular coprocessor command, and to grant full control to another thread when execution of an active thread stalls due to a long latency event, or to grant temporary control to another thread when execution of an active thread stalls due to a short latency event.

w. Add new claim 37,

37. A method of controlling the execution of instructions within an embedded processor complex which contains a plurality of protocol processor units (PPUs), each protocol processor unit containing at least two core language processors (CLPs), each CLP having at least two code threads, wherein the threads are used by each of said PPUs for executing specific tasks for the PPUs, and used by multiple logical coprocessor interfaces coupled to said plurality of coprocessors to provide access between the coprocessors and each CLP, and two arbiters between the CLPs and the coprocessors, and the step of providing instructions that enable the system to identify long latency events and short latency events according to the expected response time to a particular coprocessor command, and to grant full control to another thread when execution of an active thread stalls due to a long latency event, or to grant temporary control to another thread when execution of an active thread stalls due to a short latency event.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong N. Hoang whose telephone number is (703)

605-4239. The examiner can normally be reached on Monday - Friday 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703)305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ph
July 30, 2004

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